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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,442	12/03/2003	M. Albert Capote	90060	5385

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EXAMINER	
MALEVIC, DJURA	
ART UNIT	**PAPER NUMBER**
2884	

DATE MAILED: 12/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/725,442	CAPOTE ET AL.	
	Examiner	Art Unit	
	Djura Malevic	2884	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1- 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lingren et al. (5,786,597) in view of Spartiotis et al. (US Patent 5,952,646) and in further view of Capote et al. (US Patent 6,017, 634) and Su et al. (US Pub. 20030229986).

Regarding claim 1, Lingren discloses a radiation detector (Fig. 3a) comprising: A semiconductor detector array substrate 210 comprising: CdSnTe or CdTe 212 having a plurality of detector cells; an interposer card 214 having planar dimensions no larger then the planar dimensions of the semiconductor detector array substrate; a plurality of interconnect pads on the first surface and one readout semiconductor chip with at least one connector on the second surface wherein the semiconductor chip having planar dimensions no larger than the planar dimensions of the interposer card 214. Lingren does not expressly disclose solder columns that extend from contacts on the interposers first surface to the plurality of pads on the semiconductor detector with said columns comprising solder having a melting point less than 120 degrees C°.

Spartiotis teaches that readout cells connected to detector cells by means of low temperature solder, preferably below 120 degrees C° is a preferred method for merging

a detector and an interposer (Col. 2, Line 15). Lingren and Spartiotis are analogous art because they are both from solder bump processes.

It would have been obvious at the time the invention was made to a person of ordinary skill in the art to modify Lingren to include a detection module merged by means of low temperature solder bumps as taught by Spartiotis in order to have, increased (high) resolution, one-to-one correspondence and that the process can be prepared at a low temperature. Note that this process also facilitates an effortless alignment, which makes ease of manufacturing as well as improved performance and reliability (Col 2, Line 39).

Further regarding claim 1, Lingren does not expressly disclose an encapsulant between said interposer surface and said detector, encapsulating said solder columns. Capote teaches that encapsulation can result in significant improvements in the fatigue life of the solder bumps as compared to an unencapsulated assembly (Col 1, Line 55).

It would also have been obvious at the time the invention was made to a person of ordinary skill in the art to modify Lingren to include an encapsulation, which includes encapsulating said solder columns at a temperature no greater than 120 degrees C^{o} such as that taught by Capote in order to improve the fatigue life of the solder bumps (Col. 1, Line 55).

Further regarding claim 1, Lingren does not expressly disclose a solder barrier metallization. Su teaches that typical solder bumping processes involve a protective metallurgy layer (solder barrier metallization) [0010].

It would also have been obvious at the time the invention was made to a person of ordinary skill in the art to modify Lingren to include a diffusion barrier such as that taught by Su in order to prevent the diffusion of solder into the underlying material [0010 – 0011].

Regarding claim 2, Capote discloses that the encapsulant comprises a cured polymer (Col. 2, Line 1).

Regarding claim 3, Lingren discloses that the contact metallization comprises gold or platinum (Col. 8, Line 44).

Regarding claim 4, Su discloses the barrier layer comprising metals selected from the list that includes Ni, Au, Ti, V, and Cu [0011].

Regarding claim 5, Lingren discloses a radiation detector (Fig. 3a) comprising:

A semiconductor detector array substrate 210 comprising CdSnTe or CdTe 212 having a plurality of detector cell first surface, an interposer card 214 having planar dimensions no larger then planar dimensions of the semiconductor detector array substrate, a plurality of interconnect pads on a first surface, and one readout semiconductor chip and one connector on second surface with each having planar dimensions no larger than the planar dimensions of the interposer card 214. Lingren does not expressly disclose solder bumps on the interposers first surface to the plurality of pads on the semiconductor substrate.

Spartiotis teaches that readout cells being connected to detector cells by means of low temperature solder, preferably below 120 degrees C° is a preferred method for

merging a detector and an interposer. Lingren and Spartiotis are analogous art because they are both from solder bump processes.

It would have been obvious at the time the invention was made to a person of ordinary skill in the art to modify Lingren to include a detection module merged by means of low temperature solder bumps as taught by Spartiotis in order to have, increased (high) resolution, one-to-one correspondence and that the process can be prepared at a low temperature. Note that this process also facilitates an effortless alignment, which makes ease of manufacturing as well as improved performance and reliability (Col 2, Line 39).

Further regarding claim 5, Lingren does not expressly disclose a fluxing agent between said interposer surface and said detector. Capote teaches that a fluxing agent encapsulating the solder bumps can result in significant improvements in the fatigue life of the solder bumps.

It would also have been obvious at the time the invention was made to a person of ordinary skill in the art to modify Lingren to include an encapsulation, which includes encapsulating said solder columns at a temperature no greater than 120 degrees C° such as that taught by Capote in order to improve the fatigue life of the solder bumps.

Further regarding claim 5, Lingren does not expressly disclose a solder barrier metallization. Su teaches that typical solder bumping processes involve a protective metallurgy layer (solder barrier metallization).

It would also have been obvious at the time the invention was made to a person of ordinary skill in the art to modify Lingren to include a diffusion barrier (protective

metallurgy layer) such as that taught by Su in order to prevent the diffusion of solder into the underlying material [0010 – 0011].

Regarding claims 6, 7 and 15-17, Lingren discloses the method for making the detector array assembly as claimed in claim 5, but does not expressly disclose solder bumps and metallized detector cell pads having melting points below 120 degrees C°. Spartiotis discloses solder bumps preferably having melting points below 120 degrees C° (Col. 2, Line 44).

It would also have been obvious at the time the invention was made to a person of ordinary skill in the art to modify Lingren to include solder bumps and metallized detector cell pads having melting points below 120 degrees C° such as that taught by Spartiotis in order to avoid the need to form bumps on both the detector and readout substrates, which provide economies of manufacture as well as improved performance and reliability (Col. 2, Line 39).

Regarding claims 8 and 9, Lingren discloses the method for making the detector array assembly as claimed in claim 5, but does not expressly disclose a polymer encapsulant between the two surfaces and cured at a temperature no greater than 120 degrees C°. Capote teaches that the encapsulating composition (polymer) can be applied directly onto the surfaces of the devices that are joined electrically and mechanically within the claimed temperature (Col. 3, Line 5).

It would also have been obvious at the time the invention was made to a person of ordinary skill in the art to modify Lingren to include disclose an encapsulant between the two surfaces and cured at a temperature no greater than 120 degrees C° such as

that taught by Capote in order to improve the fatigue life of the solder bumps (Col. 1, Line 55).

Regarding claims 10 –12, Lingren discloses the method for making the detector array assembly as claimed in claim 9, but does not expressly disclose the combined unit and encapsulant continues or proceeds until said encapsulant is fully hardened.

Capote teaches that the bumped substrate (combine unit) can be coated with the fluxing composition (encapsulate) so that it effectively fluxes the soldering of the interconnections, and then also hardens to form the solid encapsulant after soldering. Capote further teaches that the heat applied during the solder reflowing operation will also harden the adhesive to create high-strength bond (Col. 13, Line 41).

It would also have been obvious at the time the invention was made to a person of ordinary skill in the art to modify Lingren to include an encapsulant between the two surfaces such as that taught by Capote in order to improve the fatigue life of the solder bumps (Col. 1, Line 55).

Regarding claim 13, Lingren discloses that the contact metallization comprises gold or platinum (Col. 8, Line 44).

Regarding claim 14, Su discloses the barrier layer comprising metals selected from the list that includes Ni, Au, Ti, V, and Cu [0011].

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wu et al. (US Patent 6,312,974) teaches a barrier layer for solder bumps and Thomas (US 20020163055) teaches a polymeric encapsulant.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Djura Malevic whose telephone number is 571.272.5975. The examiner can normally be reached on Monday - Friday between 8:30am and 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Porta can be reached on (571) 272-2444. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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